19. (amended) An apparatus, comprising:

a first processor for performing scalar processing, said first processor comprising a core, a program memory and a local memory;

a second processor for performing vector processing, said second processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said first processor to said core of said second processor;

a memory circuit for coupling said local memory of said first processor to said local memory of said second processor; and

[The apparatus of Claim 6,] wherein an instruction set is provided to said first processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions:

integers corresponding to arithmetic and logic operations on integer numbers;

transfer corresponding to the transfer operations between a register in said first processor and memory;

monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor.

36. (amended) An apparatus, comprising:

a first processor comprising a core, a program memory and a local memory;

a second processor, of a design other than said first processor, comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said [core of said] first processor to said [core of said] second processor; and

one and only one common memory coupling said [local memory of said] first processor to said [local memory of said] second processor.

37. (amended) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor, of a design other than said main processor, comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.

38. (amended) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being of a design which enables said protocol processor [suited] to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

a common memory coupling said local memory of said main processor to said local memory of said protocol processor.

39. (amended) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being of a design which enables said protocol processor [suited] to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.

IN THE CLAIMS - (clean version):

6. An apparatus, comprising:

a first processor for performing scalar processing, said first processor comprising a core, a program memory and a local memory;

a second processor for performing vector processing, said second processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said first processor to said core of said second processor; and

a memory circuit for coupling said local memory of said first processor to said local memory of said second processor.

7. The apparatus of Claim 6, wherein said second processor is the main processor of said apparatus.

8. The apparatus of Claim 7, wherein said first processor is a microprocessor.

9. The apparatus of Claim 7, wherein said second processor is a digital signal processor "DSP".

10. The apparatus of Claim 6, wherein said program memory of said first processor is ROM memory.

11. The apparatus of Claim 6, wherein said local memory of said first processor is RAM memory.

12. The apparatus of Claim 6, wherein said program memory of said second processor is ROM memory.

13. The apparatus of Claim 6, wherein said local memory of said second processor is RAM memory.

14. The apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is physically separate from said first and second processors.

15. The apparatus of Claim 6, wherein said memory circuit for coupling said local memory of said first processor to said local memory of said second processor is a DPRAM memory.

17. The apparatus of Claim 6, wherein said synchronizing circuit ensures that only one of said first and processors utilizes said memory circuit for coupling said local memory of said first processor to said local memory of said second processor, at any one time. The Asano reference fails to teach or suggest this further limitation in combination with the requirements of Claim 6.

19. (amended) An apparatus, comprising:

a first processor for performing scalar processing, said first processor comprising a core, a program memory and a local memory;

a second processor for performing vector processing, said second processor comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said first processor to said core of said second processor;

a memory circuit for coupling said local memory of said first processor to said local memory of said second processor; and

wherein an instruction set is provided to said first processor, comprising at least one field of execution conditions which is intended therefor and comprises at least the following classes of instructions:

integers corresponding to arithmetic and logic operations on integer numbers;

transfer corresponding to the transfer operations between a register in said first processor and memory;

monitoring corresponding to the monitoring of all of the operations modifying the value of an incrementation register in said protocol processor.

34. The apparatus of Claim 6, wherein said scalar processing encompasses a high-level task which is the monitoring of an application or the management of functioning and tasks which are generally carried out by hard-wired logic which are the protocol processing.

35. The apparatus of Claim 6, wherein said vector processing includes signal processing tasks generally carried out by a DSP and matrix computation which requires a more powerful structure than that of the DSP and which is generally of the array processor type.

36. (amended) An apparatus, comprising:

a first processor comprising a core, a program memory and a local memory;

a second processor, of a design other than said first processor, comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said first processor to said second processor; and

one and only one common memory coupling said first processor to said second processor.

37. (amended) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor, of a design other than said main processor, comprising a core, a program memory and a local memory;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.

38. (amended) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being of a design which enables said protocol processor to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

a common memory coupling said local memory of said main processor to said local memory of said protocol processor.

39. (amended) An apparatus, comprising:

a main processor comprising a core, a program memory and a local memory;

a protocol processor comprising a core, a program memory and a local memory, said protocol processor being of a design which enables said protocol processor to execute tasks to which the main processor is not suited;

a synchronizing circuit for coupling said core of said main processor to said core of said protocol processor; and

one and only one common memory coupling said local memory of said main processor to said local memory of said protocol processor.

REMARKS

Claim 19 stands objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. By this amendment Claims 19 has been rewritten in independent